What is claimed is:

1. A semiconductor circuit system comprising:

a first signal line; and

n circuit sections (n is an integer equal to or more than 2), each of which has an input terminal and an output terminal, and

wherein said input terminals of predetermined k ones (k is an integer satisfying $2 \leqq k < n$) of said n circuit sections are connected to said first signal line, and

said output terminal of a m-th one ($1 \leqq m \leqq n-k$) of said n circuit sections is connected to said input terminal of a (m+k)-th one of said n circuit sections.

2. The semiconductor circuit system according to claim 1, wherein each of said n circuit sections starts an operation in response to a start signal on said first signal line and stops the operation a predetermined time after the start of the operation.

3. The semiconductor circuit system according to claim 1, wherein each of said n circuit sections has a differential input circuit and a register circuit, and

said differential input circuit is activated in response to a start signal on said first signal line to start an operation and stops the operation a predetermined time after the start of the operation.

4. The semiconductor circuit system according to claim 1, wherein each of said n circuit sections has a differential input circuit and a register circuit, and

said differential input circuit is activated in response to a start signal on said first signal line to start an operation and stops the operation in response to an output from said register circuit.

5. The semiconductor circuit system according to claim 4, wherein the output from said register circuit is used as said start signal for a next one of said n circuit sections which is connected to said circuit section.

6. The semiconductor circuit system according to claim 1, wherein each of said n circuit sections comprises:

a plurality of differential input circuits;

a plurality of register circuits connected to output terminals of said plurality of differential input circuits, respectively; and

a control circuit connected with at least one of said plurality of register circuits as a specific register circuit and said plurality of differential input circuits,

wherein said specific register circuit executes a predetermined operation using a first

signal outputted from a corresponding one of said plurality of differential input circuits, and outputs a second signal to said latch circuit when the operation ends, and

said control circuit activates said plurality of differential input circuits in response to a third signal to operate and stops the operations of said plurality of differential input circuits in response to said second signal.

7. The semiconductor circuit system according to claim 6, wherein said plurality of register circuits comprises at least one set of registers and at least one set of data registers, and

said specific register circuit includes said set of registers.

8. The semiconductor circuit system according to claim 7, wherein each of said registers outputs a pulse signal to a corresponding one of said data registers when said first signal is supplied, such that data are written in a corresponding one of said data registers, and propagates said first signal to a next one of said registers which is connected to said register, and

a last one of said registers outputs said first signal as said second signal.

9. The semiconductor circuit system according to claim 6, wherein said control circuit comprises:

a first latch which latches said second signal;

a second latch which is set in response to said third signal and is reset in response to said second signal latched by said first latch; and

a switch which activates said plurality of differential input circuits when said second latch is set and inactivates said plurality of differential input circuits when said second latch is reset.

10. The semiconductor circuit system according to claim 1, wherein said n circuit sections are provided for different the semiconductor chips, respectively.

11. A semiconductor circuit comprising:

a plurality of differential input circuits;

a plurality of register circuits connected to output terminals of said plurality of differential input circuits, respectively; and

a control circuit connected with at least one of said plurality of register circuits as a specific register circuit and said plurality of differential input circuits,

wherein said specific register circuit executes a predetermined operation using a first

signal outputted from a corresponding one of said plurality of differential input circuits, and outputs a second signal to said latch circuit when the operation ends, and

said control circuit activates said plurality of differential input circuits in response to a third signal to operate and stops the operations of said plurality of differential input circuits in response to said second signal.

12. The semiconductor circuit according to claim 11, wherein said plurality of register circuits comprises at least one set of registers and at least one set of data registers, and

said specific register circuit includes said set of registers.

13. The semiconductor circuit according to claim 12, wherein each of said registers outputs a pulse signal to a corresponding one of said data registers when said first signal is supplied, such that data are written in a corresponding one of said data registers, and propagates said first signal to a next one of said registers which is connected to said register, and

a last one of said registers outputs said first signal as said second signal.

14. The semiconductor circuit according to claim 11, wherein said control circuit comprises:

a first latch which latches said second signal;

a second latch which is set in response to said third signal and is reset in response to said second signal latched by said first latch; and

a switch which activates said plurality of differential input circuits when said second latch is set and inactivates said plurality of differential input circuits when said second latch is reset.